AMENDMENTS TO THE SPECIFICATION

Please amend the specification paragraphs below to read as follows:

[0021] Fig. 5 shows another embodiment of the invention, which utilizes an optical link 108b for each data path on an optical bus 111. In this embodiment there is a one-to-one replacement of an electrical bus line which normally interconnects memory controller 104 with a memory module 113 with an optical link 108b. For simplicity, Fig. 5 only shows four such optical links (two DQ, one CMD [[of]] and a CLK path). The individual optical links 108b connect with transmitter/receivers 211 or receivers 213 on the memory modules which convert the optical signals to electrical signals for use by memory devices 112 and electrical signals to optical signals for data read from the memory devices 112.

[0024] It should also be noted that although all data paths (e.g., write/read (also referred to herein as "read/write" or "read and write") data (DQ), command (CMD), address (ADD), clock (CLK) between the memory controller 104 and modules 113 are shown as utilizing optical transmission, it is also possible to use optical transmission only on the high speed data paths, e.g., the write/read data ~~(CD)~~ (DQ) and clock (CLK) paths and utilize conventional electrical bus lines for slower speed data paths, e.g. command ~~(CMB)~~ (CMD), address (ADD).